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Digital To Analog TV Decoder design And Fabrication

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Abstract: *Digital signal transmission with its high level of immunity to signal impairments has found a wide range of applications in telecommunication systems. Digital migration came forcefully with the global deadline set by the International Telecommunication Conference as of June 2015[1],[2], inspired by limitations of analog transmission systems and the high signal strengths of the digital transmission systems. This has been of much benefit to governments and consumers.However,the shift came with its challenges; high rate of unemployment,high cost of living and high inflation levels rendering digital migration expensive. This shift makes most people especially in developing countries stillstruggle in acquiring the costly digital compliant TV sets or buying set top boxes made for digital signal conversion.Moreover, maintenance of the digital transmission standards is also costly and thus untenable due to the monthly subscription cost. A simple non programmable digital to analog decoder based on frequency shift keying (FSK) digital modulation scheme and digital to analog conversion has been designed and implemented. It consists of FSK Modulation and demodulation using PLL implemented with CD4046, serial in parallel out (SIPO) shift register 74LS164 as a multiplexer, DAC 0808 converter, LC receiver and a DC power supply.*

Keywords: *TV Decoder,FSK modulation, FSKdemodulation,phase locked loop***.**

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I. Introduction

Digital signal transmission is a powerful technology currently being used to convey information from point to point. It is widely used in many applications such as telecommunication and video speech [3].With the International Telecommunication Union Regional Radio Communication Conference(ITC-RCC-06) agreement at Geneva in 2006 to shift transmissions from analog to digital [2],[4],[5], [6].It has been necessary to adopt digital transmission due to its strengths over analog transmission. Digital signals have a higher picture quality and compression allows for bulk transmission of information [7]. Digital signals don't degrade in quality and their transmission has a broad bandwidth [8],[9]. They are clearer and suffer from minimal signal impairments,low noise levels and less attenuation[10],[11]. Digital signals have high security of information due to coding and their transmission consumes low power compared to analog signals [12].Complete digital migration involves replacement of analog signals with effective digital signals which are easy and cheaper to process and transmit [13].This move will improve the quality and quantity of programs to be viewed by the consumers [14]. For the existing analog TV sets it is therefore necessary to have signal conversion from digital to analog toenable them detect the sent information from digital transmitters in TV stations. To achieve the conversion a set top box which converts digital terrestrial television (DTT) signal for the analog TV set detection[15],[16].Most countries have successfully transited to digital unlike the third world countries where digitization process is quite expensive with a number of them still in the process of rolling out the shift [17],[18],[19],[20],[21],[22], [23].This is as a result of several challenges like cost, poverty, unemployment among others [16], [24],[25],[26], [27], [28], [29].The digital compliant TV sets are quite costly above the reach of the ordinary citizens [18],[30], [31]. The available set top boxes are based on complex technologies involving programming and thus quite a challenge for third world countries to implement such a product locally and become self-reliant. A simple reliable decoder locally made will make it simpler for most people to comply with this advanced digital technology.

Theoretical Framework

Figure 1 shows the layout of the decoder. It consists of:tuning circuit, demodulation circuit,multiplexing units and the digital to analog conversion unit. The units are powered using a power supply circuit made to step down the voltage, rectify and regulate it to ±5V,±12V and ±15V.

The tuner detects the radiation frequency broadcast and changes the carrier frequency into a fixed frequency for the next stage. In communication and transmission, reception for unguided media is achieved by means of an antenna-an electrical conductor used for radiating or collecting electromagnetic energy[12].On tuning, the antenna receives the modulated wave inform of electromagnetic wave and converts it into electrical energy fed to the demodulating circuit for demodulation.

Demodulationis a Phase Locked Loop (PLL) using FSK digital modulation scheme that shifts the frequency of the carrier signal between two distinct values [32].It replicates the original data initially encoded into the carrier by the modulator as two frequencies f_0 and f_1 at the transmission stage. The demodulator detects the two values of frequency representing a low (0) and high (1) levels of the digital data signal thus replicating the original data impressed on the carrier. It uses PLL technique of electronic frequency control widely used in communications systems[33].

The DAC is the part of the system that converts the replicated data signal into analog format detectable by the analog TV set. Most signals carrying information such as pressure, temperature, charge, current and time are available in analog form [34]. With microprocessor technology development it is necessary to process data digitally to minimize noise and for better accuracy hence the need for an analog to digital (A/D) converter [34] and a digital to analog (D/A) converter for conversion to interpretable form which is analog.

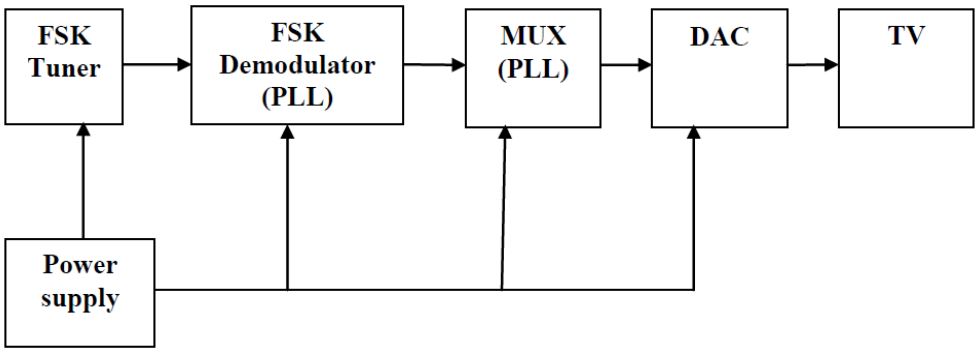

Figure 1: Block diagram of decoder.

The DAC is interfaced with the multiplexer at its input which is a serial-in parallel-out shift (SIPO) register. The register convertsthe serial digital stream into 8 bit symbols for input to the 8 bit digital converter. It has a clocking circuit for data synchronization as it flows through its flip flops and a resetting circuit to clear the flip flops to zero after maximum count of 255 (digital bits 11111111).Figure 2 shows how the DAC samples data for conversion.

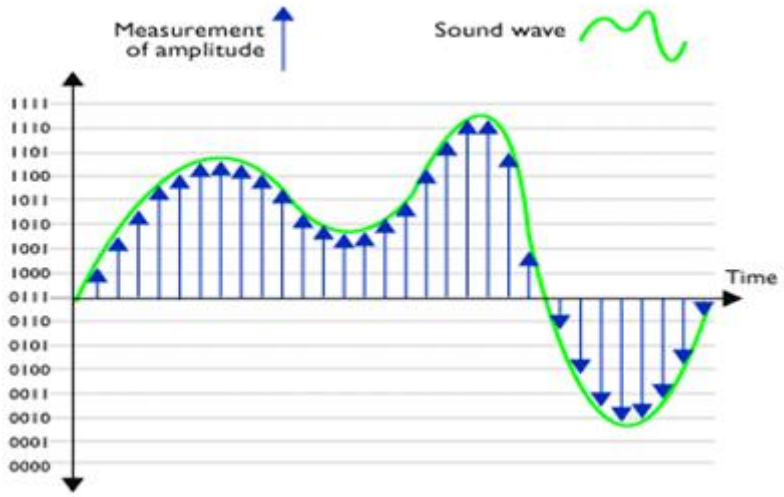

Figure2: Digital level sampling by a DAC.

The DAC alters digital codes into a concrete series of impulses that are then processed by a reconstruction filter via some method of interpolation to fill in the data between impulses[35].As per Nyquist

Shannon sampling theorem, a DAC rebuilds an original signal from a sampled data as long as its bandwidth is less than the Nyquist frequency[36].Fast Fourier Transform (FFT), a mathematical tool that relates the frequency domain of a signal to its time domain forms the basis under which the DAC part of the decoder operates [37].

Demodulation and Modulation Circuit Designs

This circuit was made using PLL - a closed feedback system whose output frequency and phase are in lock with the frequency and phase of the input signal [38].It tracks the digital signal and recovers the digital information from the digital carrier for conversion when in lock state. The hardware components were CD4046 phase locked loop, two 10kΩ and one 100kΩresistor, two 0.1µf and one 0.01 µf capacitors.Figure3 shows the design circuit. The output of the demodulator was conditioned using a low pass filter designed using a 0.01 µf capacitor and a one kΩ resistor. It was then reshaped using a comparator with a 25 kΩ variable resistor connected to the non-inverting input to set the R_1 and R_2 values.

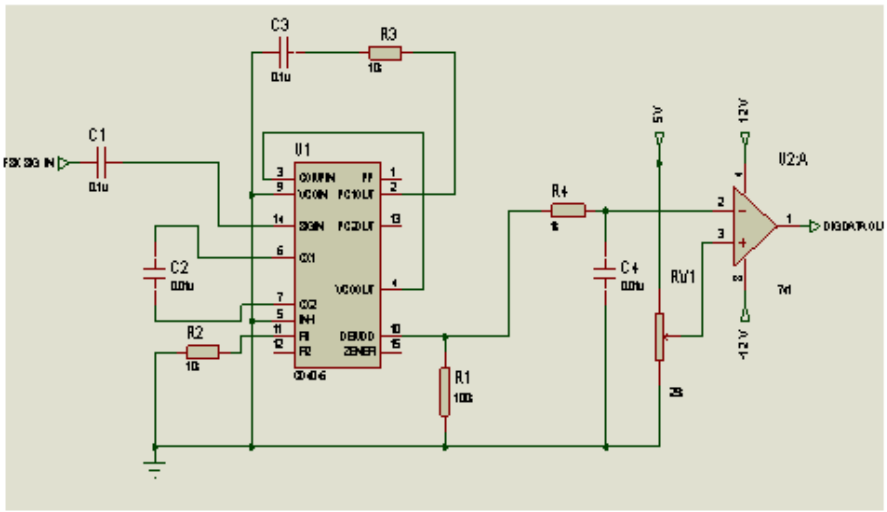

Figure3: Schematic diagram of the FSK demodulation circuit.

To test the demodulator a modulator was designed to generate FSK signal from a digital modulating wave. The hardware used included; CD4046, two 10kΩ and a 12 kΩ resistors, 0.01µf capacitor and a zenerdiode. Figure 4 shows the FSK modulation design circuit.

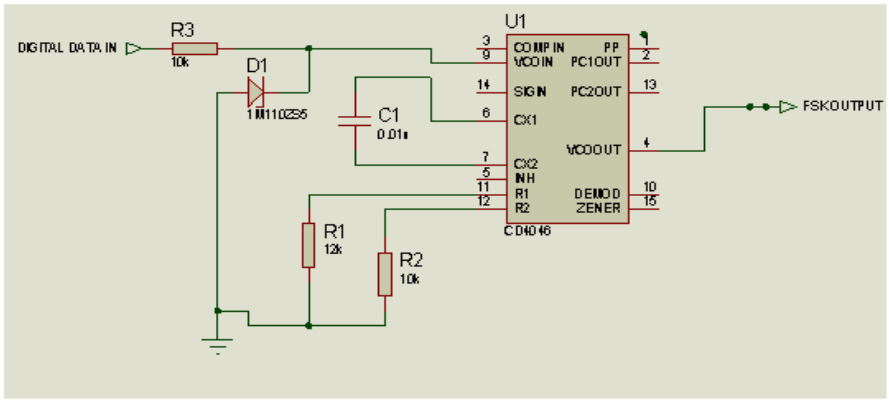

Figure 4: Schematic diagram of the FSK modulation circuit.

The PLL properties which include lock range,capture range and free running frequency can be determined using equations(1), (2), (3)and (4) [1], [3], [39].

(a) $f_L = \frac{8f_R}{V_{CC}}$ (1)

(b) $\sqrt{f_C = \frac{f_L}{2\pi RC}}$ (2)

(c) $f_R = \frac{1.2}{4R_1C_1}$ (3)

(d) $f_R = \frac{f_{max} + f_{min}}{2}$ (4)

Where f_R is free running frequency, f_C is capture range, f_L is lock range, f_{max} is maximum frequency f_{min} is minimum frequency, R_1 and C_1 are the timing resistor and capacitor values.

Tuning circuit

A tuning circuit was designed to detect free to air FSK .A LC circuit-an oscillator that can be made electrically tunable over range of frequencies [40], was designed whose values of inductor and capacitor were chosen to detect signals within the TV transmission spectrum. Figure 5 shows the design circuit of the receiver.

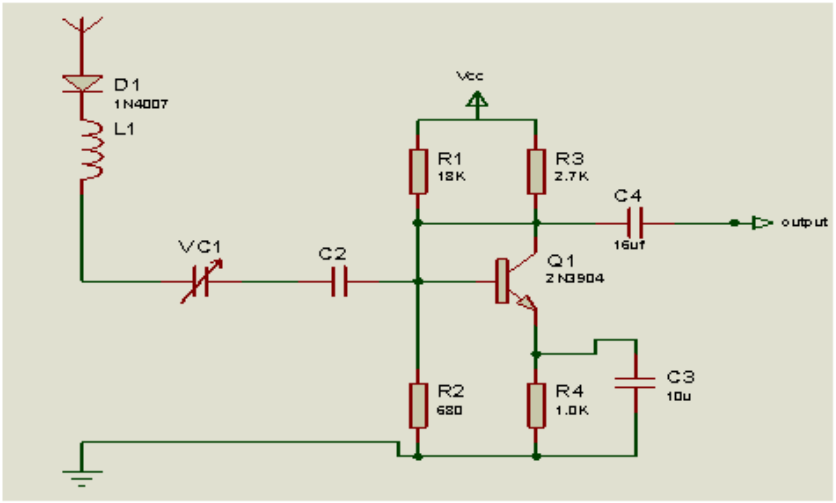

Figure 5: Schematic diagram of the LC tuning circuit.

Digital to analog converter circuit

The digital to analog decoder circuit hardware included; DAC0808, 2kΩ resistors, 0.1 µf capacitor and a 741 operational amplifier. Figure 6 shows the 8 bit data conversion circuit connection

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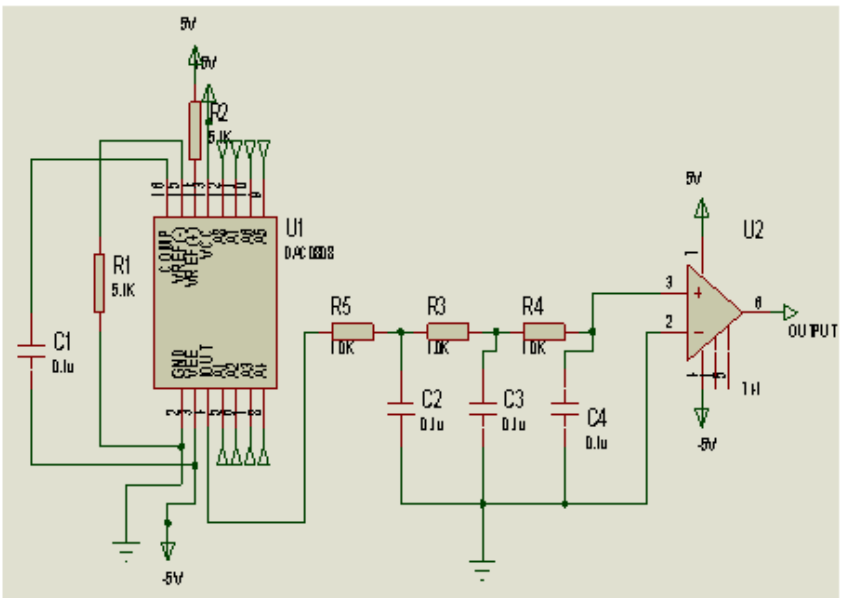

Figure 6: Schematic diagram of the 8 bit data conversion circuit.

The DAC was interfaced with a shift register 74LS164 serial in parallel out (SIPO) .74LS164 is one input eight output register that changed the serial data from the demodulator to eight pulses for input into the DAC [41]. It was clocked using NE555 timer that generated a pulse at a frequency of 64Hz for data synchronization. The timer was connected in astable mode as shown in Figure 7.In astable mode the oscillator charges and discharges indefinitely between $\frac{2}{3}V_{CC}$and$\frac{1}{3}V_{CC}$ [42]. As it switches between two states it producesrectangular waveformsthat can be used in clocking [43].Figure 7 shows the digital to analog converter interfaced with the shift register

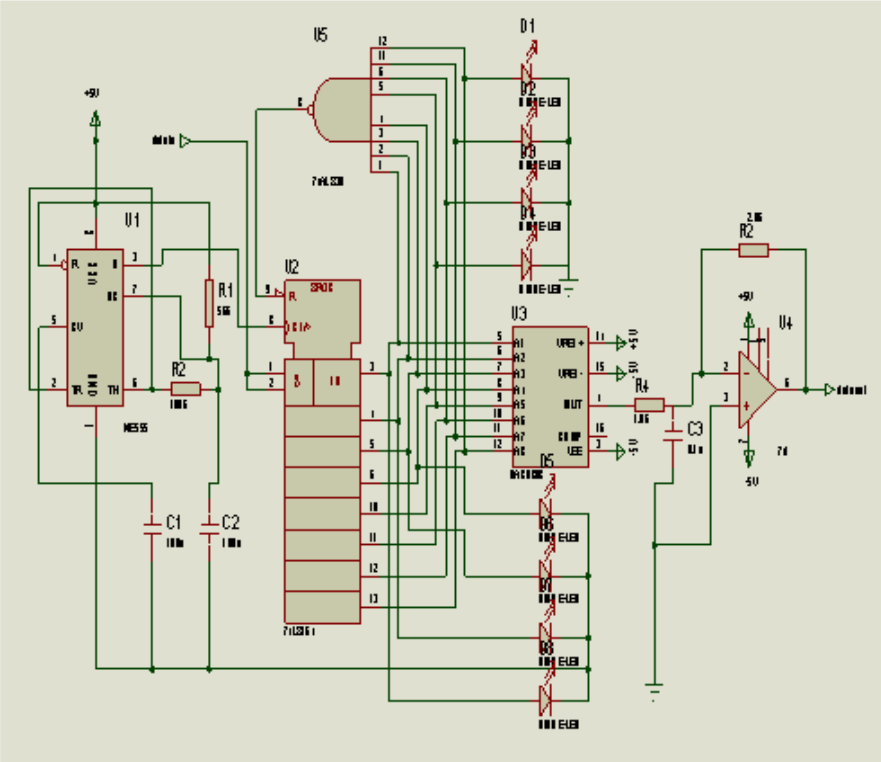

Figure 7: Schematic diagram of the shift register connected the DAC.

ANANDgate is a circuit with two or more inputs and one output, the output is HIGH if any or all inputs are LOW and LOW when all inputs are HIGH [44].NAND gate 74LS30, an eight bit one output gate was used as a resetting unit to clearing all the flip flops to a low state (00000000) after the maximum count of 255 (code 11111111).This ensures a continuous flow of data through the flip flops. Figure 8 shows all the decoder units connected to make the complete decoder design configuration.

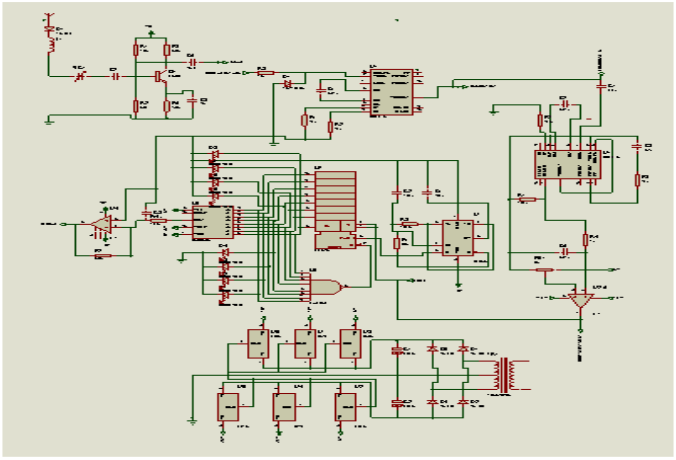

Figure 8: Complete circuit diagram of the digital to analog decoder.

II. Results And Discussion

The digital to analog decoder was tested using a digital signal from a digital generator at a frequency of 92 Hz. This was modulated using FSK at a modulating frequency of 4 KHz and 8

KHz at a central voltage controlled oscillator (VCO) frequency of 6KHz and then demodulated for conversion into analog form. Plates 1(a), 1(b) and 1(c) show a correlation of input and output signals from the decoder units at every stage.

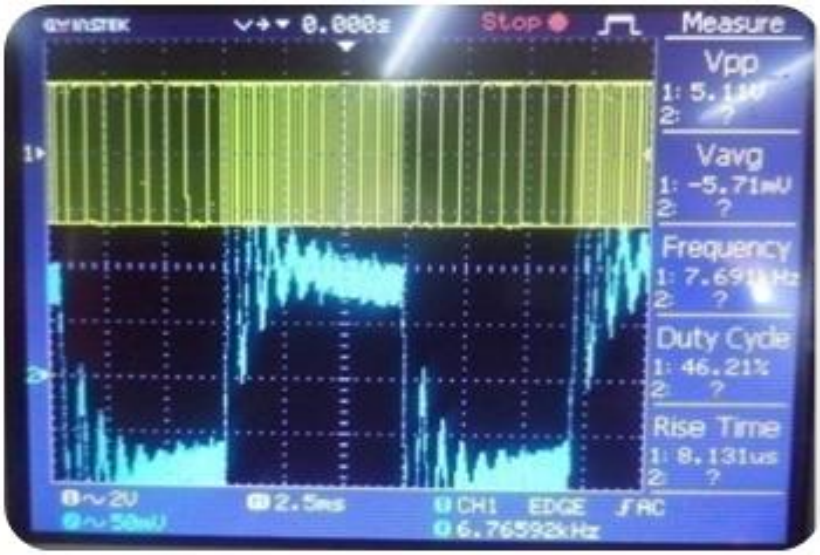

Plate 1 (a): Obtained FSK signal at a frequency of 4 KHz for the low bit and 8KHz for the high bit compared to the demodulated digital signal before filtering.

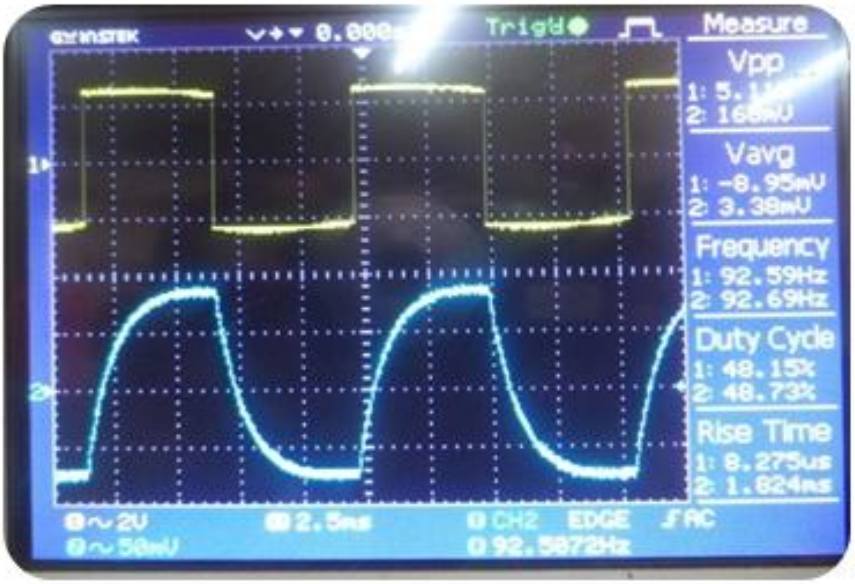

Plate 1 (b): **Input digital signal at a frequency of 92.59 Hz compared to the digital signal from the demodulator output** after filtering and before signal conditioning

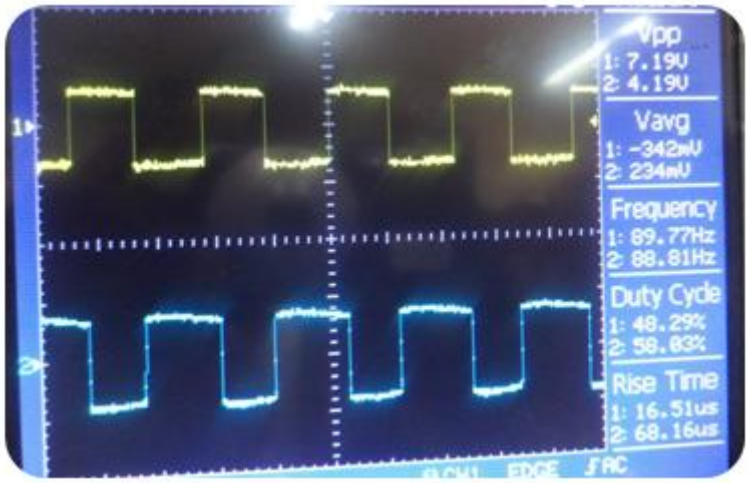

Plate 1(c): Input digital signal compared to the demodulator output digital signal after signal conditioning as tapped from the comparator inverting terminal.

Figure 9 shows a comparison graph of the analog signal outputs in form of voltages against the corresponding digital signal codes. A linear model was obtained with an r square value of 0.99706 with a deviation of 0.00294 from the ideal model fit value of 1 and a standard deviation of 0.55864.The decoder is therefore gave a monotonic transfer of signal.

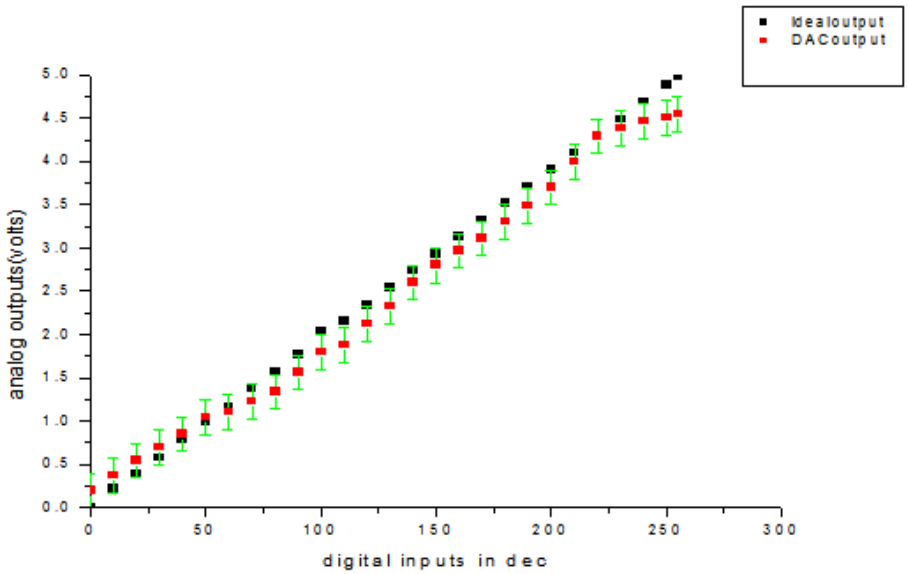

Figure 9: A correlation between the analog outputs to the digital inputs of the decoder.

Integral non-linearity (INL) and differential non-linearity (DNL) are the main specifications used to define the linearity accuracy of the DAC part of the decoder. To determine the decoder linearity and monotonicity, a linear model was fitted as shown in figure 9 that gives the transfer function of the decoder as a straight line. In determining the goodness of the fit, the regression analysis done gave a higher value of 0.99706 implying good variation of the decoder analog output to the ideal digital input codes. R squared value of 0 indicates no variation of the response while 1 indicates an ideal agreement of the model with the various responses. In this case the empirical ideal line was close to the best fit showing a monotonic data transfer of the decoder from digital to analog format.

The standard deviation shows how spread data is from the expected values. It indicates the normal and the extreme values from the mean. It is a characteristic of the non-linearity error where larger values imply large INL and DNL errors in data transfer. The decoder DAC had a small standard deviation showing good spread of the output analog voltages corresponding to the digital input values.

III. Conclusion

A non-programmable digital to analog decoder has been designed and presented which is based on FSK modulation and demodulation scheme using PLL and signal conversion using digital to analog converter. It was tested by designing a modulation circuit to generate an FSK signal currently absent in Kenyan free to air transmissions.The modulator had a free running frequency of 6KHz which was modulated to 8KHz and 4KHz frequencies for high and low digital bits respectively. The demodulator had a free running frequency of 6KHz at a lock range and capture of ±9.6KHz and ±3.6KHz respectively. The serial data was shifted parallel to the data converter that had a resolution of 0.39%,integral nonlinearity and differential non linearity of 0.023V and 0.039V respectively. It had an offset error of 0.2V and a maximum output voltage of 4.55V with 5V power supply. The decoder had a r squared value of 0.99706 and standard deviation of 0.55864 giving a linear transfer of the digital coded data into analog voltage pulses. The decoder showed good spread of data and a monotonic output where increase in digital input value led to a corresponding increase in analog output value.

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